IN THE CLAIMS

Claim 1 (Currently Amended): A clock divider of a DLL (delay locked loop), comprising:

clock dividing means for receiving a source clock of the DLL to generate a plurality of divided clocks each having a period different from each other;

test mode clock providing means for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal and a test mode period selecting reference signal; and

normal mode clock providing means for outputting selected one of the plurality of the divided clocks in a normal mode in response to the test mode signal.

Claim 2 (Currently Amended): The clock divider of the DLL as recited in claim 1, wherein the test mode clock providing means includes:

decoding means for decoding ~~address signals~~ the test mode period selecting reference signal in response to the test mode signal to generate a test mode period selecting signal; and

test mode clock selecting means for outputting one of the plurality of the divided clocks in response to the test mode period selecting signal.

Claim 3 (Original): The clock divider of the DLL as recited in claim 1, wherein the normal mode clock providing means includes:

normal mode clock option processing means for receiving the plurality of the divided clocks to output a divided clock that is fixed depending on an option; and

switching means for outputting the fixed divided clock from the normal mode clock option processing means in response to the test mode signal.

Claim 4 (Currently Amended): The clock divider of the DLL as recited in claim 2, wherein ~~the address signals are~~ the test mode period selecting reference signal is inputted through a predetermined number of address pins in the test mode.

Claim 5 (Currently Amended): The clock divider of the DLL as recited in claim 4, wherein the decoding means includes:

a plurality of NAND gates, each for receiving the test mode signal and at least one of ~~the address signals inputted to~~ a plurality of input signals inputted to the address pins and inverted signals of ~~the address signals~~ the plurality of input signals; and

a plurality of inverters for inverting a plurality of output signals outputted from the NAND gates, respectively.

Claim 6 (Previously Amended): The clock divider of the DLL as recited in claim 5, wherein the test mode clock selecting means includes a plurality of transfer gates for outputting the divided clock under control of outputs of the plurality of inverters, respectively.

Claim 7 (Original): The clock divider of the DLL as recited in claim 3, wherein the normal mode clock option processing means includes one of a fuse option, an anti-fuse option and a metal option.

Claim 8 (Original): The clock divider of the DLL as recited in claim 3, wherein the switching means includes a transfer gate that is controlled by the test mode signal.